Side Channel: Bits over Interference

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ABSTRACT

Interference is a critical issue in wireless communications. In a typical multiple-user environment, different users may severely interfere with each other. Coordination among users therefore is an indispensable part for interference management in wireless networks. It is known that, coordination among multiple nodes is a costly operation taking a significant amount of valuable communication resource. In this paper, we have an interesting observation that by generating intended patterns, some simultaneous transmissions, i.e., "interference", can be successfully decoded without degrading the effective throughput in original transmission. As such, an extra and "free" coordination channel can be built. Based on this idea we propose a DC-MAC to leverage this "free" channel for efficient medium access in a multiple-user wireless network. We theoretically analyze the capacity of this channel under different environments with various modulation schemes. USRP2-based implementation experiments show that compared with the widely adopted CSMA, DC-MAC can improve the channel utilization efficiency by up to 250%.

Categories and Subject Descriptors

C.2.1 [**Computer Communication Networks**]: Network Architecture and Design–*Wireless Communication*

General Terms

Design, Experimentation, Performance

Keywords

Wireless Network, Interference, Coordination

1. INTRODUCTION

Radio interference is a major concern in wireless communications [19] [28]. The capacity of a wireless channel highly depends on the ratio between the signal power of the desired transmission to the combined interference plus the noise (SINR) [12]. Because of the broadcast nature of wireless communications, when two or more transmissions are conducted in vicinity, mutual interference will be generated and collisions may happen.

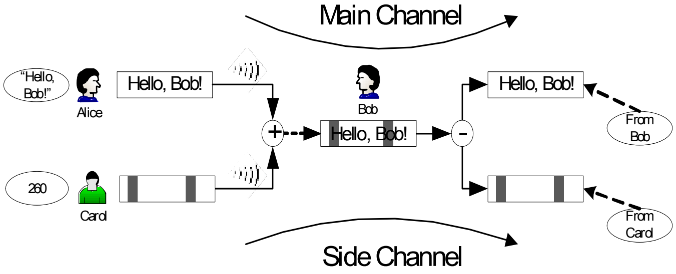

Figure 1: An example of Side Channel

In recent years, many research efforts have been devoted to the interference management. For instance, interference avoidance (e.g., CDMA, TDMA, FDMA, CSMA/CA) attempts to scatter the multiple transmissions along temporal, spatial and frequency dimensions to mitigate severe interference. Interference cancellation techniques [7, 29] try to recover the transmission errors that are due to the interference. The interference alignment and cancelation (IAC) [32] is developed to overcome the antennas-per-access point (AP) throughput by coordinating multiple APs.

In a typical multi-user environment, coordination among different users is a necessity to avoid severe mutual interference and well utilize the shared medium. Such coordination costs precious communication resource, and leads to a significantly degraded network performance.

In traditional approaches, the coordination is addressed in an either in-band or out-of-band manner. For in-band approaches, the coordination traffic stays in the same communication channel as the data traffic, bringing a large amount of communication overhead such as the Distributed Coordination Function Interframe Space (DIFS), Short Interframe Space (SIFS) and random back-offs in CSMA [2]. The out-of-band approaches are typically designed for multiple radio systems (e.g., [10]). These approaches, usually, dedicate one complete radio (and its associated channel resource) for coordination, and thus generate extra costs.

A fundamental and interesting question is, whether we can coordinate among multiple nodes without significantly wasting system resource. For this question, a promising ob-

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servation is that most physical layer implementations provide a certain level of tolerance to the radio interference. This tolerance is, however, under-utilized in many real environments. A user can exploit this redundant tolerance to transmit a small amount of control information by intentionally emitting patterned interference when other users are conducting their normal data transmission. As the current hardware is able to identify such intended patterns [13], a receiver simply recognizes these patterns and obtains the control information carried in the patterns. As such, an additional channel is built without affecting the transmission throughput in the original channel. It can be used to deliver the coordination information among users in a "free" manner. It is worth pointing out that "free" here means no degraded throughput of the original data channel. As some interference will be intensionally introduced, the original data channel will lose certain degree of the interference-tolerance capability, and this is the cost of the additional channel. Notice that we will use this additional channel for control purpose. The used bandwidth is far from its full potential. In other words, only a very small portion of the interference-tolerance capability will be sacrificed. We will give more details of this in Sec. 3. In the remainder of this paper, we call this "free" channel as Side Channel, and the original channel as the Main Channel.

For ease of understanding, we illustrate the idea of Side Channel by an example in Fig.1. In this example, Alice sends a message to Bob in the Main Channel using the conventional communication scheme. At the same time, Carol also wants to deliver some coordination information to Bob. Carol will emit intended interference patterns to Bob. The interference is strong enough so that Bob can identify its pattern, while weak enough so that the Main Channel traffic will not be corrupted. From Bob's perspective, he is not only able to successfully decode the "Hello, Bob!" message from Alice, but also notices that the interference in the packet has certain patterns. With a pre-designed protocol, Bob will be aware that it is Carol transmitting some coordination information to him. Different from the out-of-band approaches, Side Channel is an "in-band" channel that resides in the same spectrum band of the original Main Channel. Each individual antenna can independently benefit from the efficient usage of Side Channel. Different from the traditional in-band approach, no extra coordination overhead is needed by leveraging such a Side Channel.

To demonstrate the effectiveness of Side Channel, we design a new DC-MAC protocol. In DC-MAC, Side Channel is used to coordinate the data transmissions on the Main Channel. As such, there is no need to perform the random back-off, a typical distributed coordination mechanism, in the Main Channel. Notice that the back-off is one of the major sources of the communication overhead. We implement Side Channel and DC-MAC on the USRP2 platform [9]. The experimental results show that DC-MAC can dramatically improve the network throughput by up to 250% compared with CSMA.

It is, however, not straightforward to build a Side Channel and use it efficiently. Several key challenges arise during the design. The first major challenge is to carefully tune the intended interference patterns such that it can carry information without ruining the Main Channel communication. The second challenge is to derive the theoretical upper bound of the Side Channel capacity and how much we can approach this bound in a practical environment. The third challenge is to efficiently design DC-MAC so that it can fully benefit from the free coordination mechanism. Many practical issues are involved during the development, such as microsecond-level time synchronization, interference-tolerance design in Side Channel, and real-time transmission scheduling using software radio devices. We summarize main contributions of this paper as follows.

- We exploit the error patterns in physical layer and for the first time build Side Channel. It can be used in conjunction with Main Channel without degrading the effective transmission throughput in Main Channel.
- We give a complete theoretical analysis on the performance of Side Channel. Based on 802.15.4 ZigBee standard (which has a maximum throughput of 250 Kbps), we designed two modulation schemes with the theoretical capacity of 129 Kbps and 15 Kbps, respectively. Our USRP2-based implementation show that the real bandwidth can be up to 111.76 Kbps under the first scheme in the experiments.
- Based on Side Channel, we design a new DC-MAC protocol. DC-MAC aggressively schedules the transmissions on Main Channel and leverages Side Channel for control and coordination purposes. Compared with the original CSMA, DC-MAC eliminates the back-off, carrier-sense and guarantees the collision-free transmission even when the network is saturated.
- We implement Side Channel and DC-MAC in a prototype system of seven nodes using GNU Radio testbed. Comprehensive experiments show that DC-MAC can enhance the network throughput by up to 250% under the same fairness performance compared with the conventional CSMA.

The rest of this paper is organized as follows. Some preliminaries and background information is given in Section 2. This is followed by the detailed design and analysis of Side Channel in Section 3. In Section 4, we present DC-MAC design with the implementation of Side Channel and DC-MAC in Section 5. Experimental evaluations will be given in Section 6. A brief overview on the related literature is given in Section 7. Some issues in our current Side Channel design is discussed in Section 8. At last, we draw a conclusion and give some suggestions on future research.

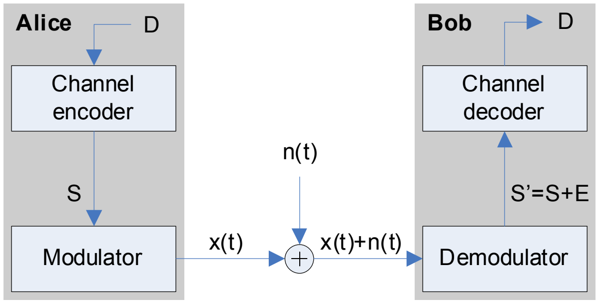
2. SYSTEM ARCHITECTURE AND PRELIMINARIES

In this section, we will describe the overall architecture in a Side Channel enabled communication system. We will also give some background knowledge of the physical layer standard that we adopt in our work.

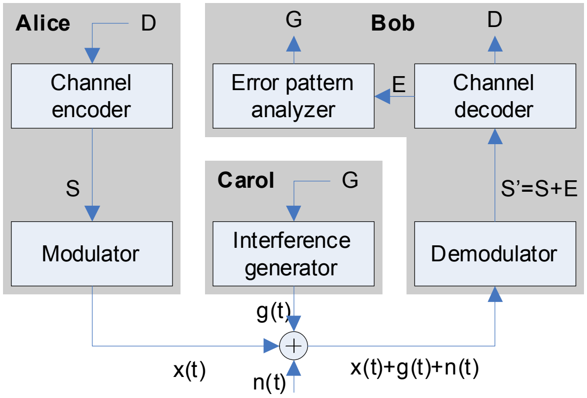
2.1 Overall System Architecture

Side Channel is based on a simple yet interesting observation that extra useful information bits can be transmitted together with the normal traffic by generating intended interference patterns.

Fig.2 (b) depicts the architecture of this new communication system with Side Channel enabled. Comparing with the traditional communication architecture in Fig.2(a), we add



(a) Illustration of the traditional communication



(b) Illustration of the Side Channel-enabled communication

Figure 2: Schematic with and without Side Channel; $x(t)$ is the signal encoded from Alice's data D; $n(t)$ is the white noise including external interference; and $g(t)$ is the intended interference that carries Carol's information G

some new modules including an intended interferer with an interference generator and an error pattern analyzer in the receiver. The Side Channel-enabled communications will work as follows. The sender in Main Channel works the same as traditional. Carol, the sender in Side Channel, will encode its data G by the interference generator and send it to the air. At the receiver end, after demodulation, the received signal S' contains signal S from Alice and error pattern information E. By using the channel decoder, Bob can get the data D from Alice. At the same time, he can conduct the error pattern analyzer to decode G from E. Thus, he can get the information D from Alice in Main Channel and G from Carol in Side Channel.

In a Side Channel-enabled communication system, several key questions are raised. Specifically, how to design interference pattern in interference generator, how to recognize error pattern by the error pattern analyzer, how much information we can deliver and how to benefit from this extra delivered information. We will answer all these questions in the later of this paper.

In the next subsection, we will begin our discussion from presenting the physical layer implementation we adopt in this work.

2.2 Background of IEEE 802.15.4

For ease of presentation, we present the design of Side Channel based on IEEE 802.15.4 ZigBee standard which is widely used in Wireless Sensor Networks [1, 14, 18, 20]. We select IEEE 802.15.4 for its simplicity and it is a typical redundant coding scheme (DSSS based). IEEE 802.11b is also based on DSSS, and thus the Side Channel design is the same. We will discuss how to extend our Side Channel design to other other physical layer standard (e.g., OFDM) in Section 8. Zigbee employs Direct-Sequence Spread Spectrum (DSSS) at the physical layer (PHY) to resist radio interference and noise. In the 2.4GHz worldwide band, an m-bit data packet $D \in \{b_i\}^m$ will be chopped into symbols $D \mapsto S \in \{s_j\}^{m/4}$. Each symbol S will be mapped to one of the 16 predefined n-bit chip[1] sequences. That is $S \mapsto X \in \{x_k\}^n, k \in [1, n]$, where n is equal to $8m$. The chip sequence X is then modulated to the radio frequency $x(t)$ and then sent to the wireless medium. For example, in IEEE 802.15.4, every 4-bit is encoded into a 32-chip sequence, corresponding to $m = 4$ and $n = 32$ ($n = 8m$).

At the receiver end, the signal will become $x'(t) = x(t) + n(t)$. Here $n(t)$ is the noise which may also include external interference. Upon getting the signal, the receiver demodulates it to the chip sequence X'. The receiver will correlate the received sequence X' with each of the 16 desired chip sequences and select one with the minimum number of bit differences and map it back to D'. The chip errors E_X is defined as $E_X = X' \oplus X$ and the symbol error E_S is defined to be $E_S = S' \oplus S$ where $\oplus$ is the XOR operation of two binary sequences. When $S = S'$ (i.e., $E_S = \{0\}^{m/4}$), we will have $D' = D$ and claim that the packet D is successfully transmitted.

3. SIDE CHANNEL DESIGN

In this section, we will present the general idea of Side Channel and identify the the situations to which it can be safely applied. Next, we propose two Side Channel modulation schemes which are suitable for different precision of time synchronization. The Side Channel capacity under these two modulation schemes will be given as well.

3.1 Design Principles of Side Channel

In this part, we discuss the design principles of Side Channel. The main issue is to find out the conditions under which Side Channel is nearly harmless to the performance of Main Channel in terms of Packet Reception Rate (PRR), and thereby can be safely used. To this end, a key parameter h, which is the maximal number of chips per symbol that we can safely interfere, will be calculated for different Main Channel conditions. Table 1 lists some notations and concepts that will be used in this paper.

In order to be safe, the joint effect of intended interference and noise should not go beyond the error correction capability (ECC) of Main Channel. To this end, we first use Symbol Error Probability (SEP) to measure quality of the Main Channel transmission. It is defined as the probability that the symbols will be incorrectly transmitted over a transmission. Assuming each symbol error will result in a packet error, the relation between SEP and the Packet Reception Rate (PRR) is shown in Fig. 3 where the left axis is

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[1] Chip is a binary representations in a lower layer than the information bits. We do not use "bit" to avoid confusion.

Table 1: Concepts and notations

Bit b_i	The information bit in data packet
Symbol s_i	Every 4 bits are encoded as a symbol
Chip x_i	The physical layer data representation unit; and only 16 sequences of 32 chips are used to represent symbols and other are unused;
SEP	The symbol error probability
f/f^{-1}	An encoding scheme $f : \{s_i\}^m \rightarrow \{x_i\}^n$, f^{-1} is its corresponding decoding
$\delta(f)$	The error correction capability of an encoding/decoding scheme
h	The maximal number of chips that can safely be interfered in a symbol
K	The number of actually interfered chips per symbol

the SEP and the right one is the corresponding PRR. For example, if PRR is required to be above 99.8%, then the desired SEP should be less than 10^{-6}.

The SEP depends on many factors. The first one is the ECC of the encoding/decoding scheme applied by Main Channel. The ECC is defined as follows.

Definition Given an n-bit binary vector $E = \{e_i\}^n, e_i \in \{0, 1\}$, we define its hamming weight $W(E)$ as the number of 1s in E, i.e., $W(E) = \sum_{i=1}^{n} e_i$

Definition Given an encoding/decoding scheme f/f^{-1},

$$\begin{aligned} f &: \{s_i\}^m \rightarrow \{x\}^n \\ f^{-1} &: \{x\}^n \rightarrow \{s_i\}^m \end{aligned}$$

its error correction capability $\delta(f)$ is defined as the maximal number of chip errors that f can correct, i.e.,

$$\delta(f) = \max(W(E_c))$$

where $E_c \in \{E | f^{-1}(f(S) \oplus E) = S, \forall S \in \{s_i\}^m\}$.

According to the encoding/decoding theory, $\delta(f)$ of a given f/f^{-1} is the half of the minimal Hamming distance between any pairs of the encoded binary vectors by f, i.e.,

$$\delta(f) = \left\lfloor \tfrac{1}{2} \min(W(f(u) \oplus f(v)), \forall u, v \in \{s_i\}^m) \right\rfloor$$

According to the current symbol mapping scheme in IEEE 802.15.4, the shortest Hamming distance between any two valid 32-Chips is 13. In other words, its $\delta(f)$ is 6.

The second influential factor of SEP is the Signal-to-Noise-Ratio (SNR) of the channel. This factor has a direct connection with chip error probability, which is defined as the probability that a chip is interfered to be an erroneous one at the receiver side. Notice that the interference is independent to the state of the original chip, and therefore the upper limit of chip error probability is 0.5 regardless that it is due to the white noise or the intended interference. We use P_N to denote the chip error probability caused by the noise (including unintended external interference) and P_I denote that caused by the intended interference patterns $g(t)$. According to digital communication theory [12], we have

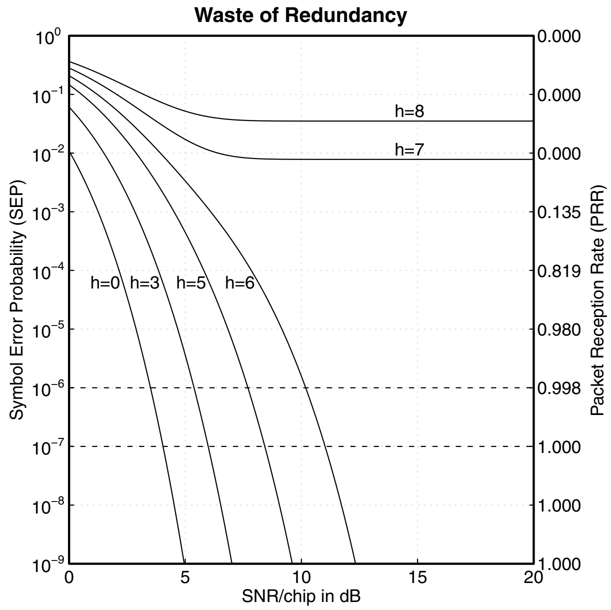

Figure 3: The relation between the number of intended interfered chips h, SEP and the PRR, assuming each packet has 2000 symbols (1000 bytes).

$$SEP = \sum_{j=\delta(f)+1}^{n} \sum_{r=0}^{h} \binom{h}{r} P_I^r (1-P_I)^{h-r} \binom{n-h}{j-r} P_N^{j-r} (1-P_N)^{(n-h)-(j-r)} \quad (1)$$

Here n is the number of chips per symbol. Setting $n = 32$, $\delta(f) = 6$, P_N and P_I to their upper limit 0.5, we investigate the impact of number of interfered chips per symbol h that varies from 0 to 8. We depict Equ. 1 in Fig. 3 and have following observations.

First, h should never exceed $\delta(f)$. Otherwise, the PRR will be dramatically decreased, leading to a severe degraded Main Channel performance. For instance, PRR is nearly 0 when $h = 7$. Second, when the channel condition is excellent (e.g., $SNR > 15dB$), h has a minor impact on the Main Channel performance as long as $h \leq \delta(f)$. In that case, we can set $h = \delta(f)$ to fully exploit the Main Channel tolerance capability and maximize the capacity of Side Channel. Third, when the channel condition is intermediate, we can exploit certain degree of the interference tolerance, leaving others for noise. For example, when SNR is around 6dB and 99.8% PRR is desired, setting $h = 3$ is an attractive option. At last, in the extreme case of very poor channel condition, Main Channel will strive to recover the transmission errors. In that case, the employment of Side Channel may not be an appropriate option.

In the next subsection, we will design Side Channel and set its parameters based on the above observations.

3.2 Modulation/Demodulation Schemes

In this subsection, we present the modulation and demodulation schemes for Side Channel transmission, i.e., the interference patterns representing data on Side Channel. We first present the main challenges during the design, and then propose two modulation schemes, namely Pulse-Position Modulation (PPM) and Pulse-Interval Modulation (PIM). The Side Channel capacity under the two modulations will be given as well.

3.2.1 Challenges in modulation scheme design

There are several main practical challenges during the modulation scheme design. First, interference does not necessarily induce chip error, as mentioned in Section 3.2 that P_I is upper limited by 0.5. Therefore, the probability that a single interfered chip become erroneous is very low (< 0.5). However, if a number of consecutive chips are interfered, then the probability that some of the chips become erroneous would be high. The natural question in the design is: how many consecutive chips should be interfered?

Another challenge is the time synchronization among multiple users. When the sender and the interferer can be chip-level synchronized, information can be represented by interfering different positions in a 32-chip symbol. It allows more information to be carried. In real wireless networks, however, chip-level synchronization may be hard to implement due to the hardware constraint. In that case, other interference patterns are desired.

According to different synchronization granulations, we design two different modulation schemes for different hardware environments, leaving more design options for future work. When the chip-level synchronization is available, PPM is suitable as having a much higher channel capacity in Side Channel. Otherwise, PIM is suggested which has more tolerance to the unsynchronized time but a lower data rate.

3.2.2 PPM design

The core idea of PPM is to represent data by interfering chips at different positions. As illustrated in Fig. 4, the 32 chips in each symbol are divided into several groups and each group contains K consecutive chips (thus $\lfloor 32/K \rfloor$ groups per symbol). For each symbol, the interferer interferes chips in one group at most. When the receiver receives the data in Main Channel, by checking which group is interfered, it can interpret the carried information.

Then we give a theoretical analysis on the Side Channel capacity under PPM scheme. When PPM is adopted, Side Channel can be formed as an M-ary erasure channel where $M = \lfloor 32/K \rfloor$. Assume a pattern with K interfered chips can be identified when at least 2 out of K chips are successfully interfered with chip error. Let P be the probability that the receiver identifies there is a pattern in the symbol. We have

$$P = 1 - (1 - p_I)^K - K p_I (1 - p_I)^{K-1}$$

where P_I is the chip error probability of interference patterns. And the channel capacity C can be calculated as

$$\begin{aligned} C &= P \log M/T \\ &= (1 - (1 - p_I)^K - K p_I (1 - p_I)^{K-1}) \log\lfloor 32/K \rfloor / T \end{aligned} \tag{2}$$

where T is the duration of one symbol. The duration T can be calculated by the Main Channel's data rate. In order to maximize the transmission reliability of Side Channel, we set the parameter K as the maximal of $K = 6$. Assuming we have the optimal Main Channel in which P_I is equal to its upper limit of 0.5, we have the corresponding channel capacity $C(K = 6, P_I = 0.5) = 129$ Kbps.

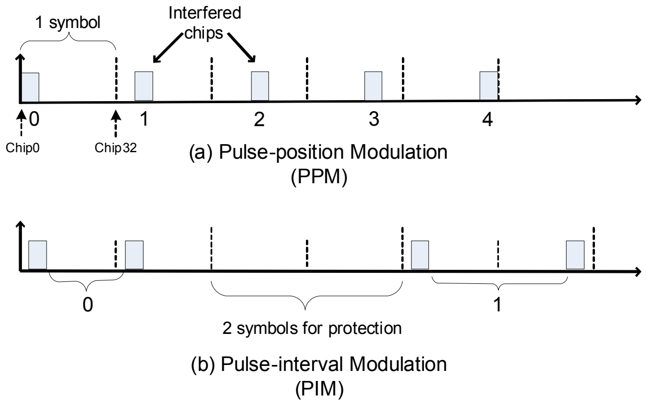

Figure 4: Modulation Schemes for Side Channel (a)Different positions encode to different information. (b)Different intervals encode to different information.

3.2.3 PIM design

The PPM has an assumption that chip-level synchronization between nodes is available. For systems of no such support, we propose another modulation scheme PIM. The core idea of PIM is to use the relative positions of interfered chips rather than the absolute positions. The information is represented by different intervals between two consecutive interfered chips. As such the requirement on the time synchronization between users can be released. Notice that though it is hard to synchronize the behaviors of the interferer and the receiver, behaviors of a single entity is easily controlled, and therefore the relative positions of two consecutive interfered chips will be kept un-changed at the receiver end.

As illustrated in Fig. 4, in PIM messages are encoded in every four symbols. Again each interference will interfere K chips to increase the reliability of the interference patterns being identified. This interference will be repeated in a consecutive symbol, while the interval between the two groups of K chips will be adjusted according to the different information being encoded. After these two symbols being interfered, two immediately followed symbols will not be interfered to provide protection.

To analyze the Side Channel capacity using PIM, assume that the first group of interfered K chips starts at chip 0. We set $K = 8$, with 2 additional chips for protection. And the second group of interfered chips must be at lest in the second symbol. To provide protection, only a limited number of position are valid for this group of interfered chips. The first possible position is 0, and $2K$ consecutive positions will become exclusive. Therefore the second possible position is only 17, and the third one is 34 which is not valid as it exceeds 32. In other words, Side Channel with PIM has only 2 states in 4 symbols in PIM. Accordingly, the data rate of PIM scheme under ZigBee is $log2/4T = 15$ Kbps.

3.2.4 Demodulation scheme design

The demodulation on Side Channel is even more challenging than modulation. It is not simply a reverse of modulation, but a process that infers the interference patterns that are intendedly generated, according to error patterns recognized. The design choices of demodulation are mainly affected by two factors. First, there is a high probability that the intended interference does not cause any chip error even when a large number of consecutive chips are intendedly interfered. Second, error patterns may also be caused by external interference or noise. Such error patterns should not be considered as the information delivered over Side Channel. These two factors lead to two categories of demodulation error: false negative and false positive. Unfortunately, none of them can be completely avoided. False negative can be considered as a data erasure on Side Channel. It can be largely mitigated by repeating the coding, e.g., generating the same intended interference pattern for several times. False positive, however, is more challenging. It is more likely to happen when the condition of Main Channel is poor. In such cases, we can hardly make use of Side Channel. For most cases, if there is only one erroneous chip in a large number of consecutive ones that are intendedly interfered, it would be safe to consider it as a false positive one. This simple yet efficient method is applied to the above two modulation schemes.

4. DC-MAC PROTOCOL

In this section we will demonstrate how to leverage Side Channel to benefit the design of multi-user medium access control (MAC) protocol. We will first outline the design principles and give an overview of the DC-MAC, followed by the details.

4.1 DC-MAC Principles and Overview

Targeting at a more efficient usage of the wireless medium, DC-MAC is design for a higher network throughput on provision of fairness among different users. For these goals we have the following observations. First, Main Channel should be aggressively accessed by the data transmission. The overhead such as the carrier-sense, DIFS, SIFS and random back-offs is of no benefits for the network throughput. Second, collision-free is highly desired so that every data packet provides a net gain. Third, the fairness is important in the sense that different users can get a similar amount of opportunities to access the medium. Fourth, collisions in Side Channel (e.g., two users try to use Side Channel simultaneously) will lead to a severe consequence. Though single intended interference may not ruin Main Channel communication, an accumulated one may too strong that corrupt Main Channel. It therefore should be largely avoided, if a guarantee is impossible.

DC-MAC is designed for the infrastructure mode which accounts the dominating portion of the nowadays wireless networks [4]. In the infrastructure mode, there is Access Point (AP) and the other associated nodes as clients. Communications in Main Channel are only conducted between Clients and AP. We refer a communication session from the AP to Clients as download, and the reverse one as upload. Both upload and download are called *communication*. In each communication, there are two transmitting *operations*, one for data and the other for the acknowledgement. A transmission operation from the AP to the Clients is called downlink, which can either be for data or for acknowledgement. The reverse direction operation, called uplink, is similar.

Fig. 5 gives an example of DC-MAC operations in time series. It involves four nodes, namely the AP, Clients A, B and C, and two communications, one upload and one download. In DC-MAC, only the AP functions as the Side Channel "receiver" (Bob in the example of Fig. 1). The transmission operations are placed consecutively along the time dimension with no gap in between, and the two kinds of operations uplink and downlink are alternately scheduled. During an uplink in an upload communication, and the uplink in certain download communications, Clients are allowed to send their request to the AP through Side Channel. Notice that these requests are for upload communications only, and the download are from the external networks and need no request. The AP collects the requests, schedules them on the time dimension and places them in Main Channel. In DC-MAC, the AP is responsible for the provisioning of the fairness. The Clients should response to AP's coordination. In the next, we will give a more detailed description of DC-MAC from the AP and Client's perspectives respectively.

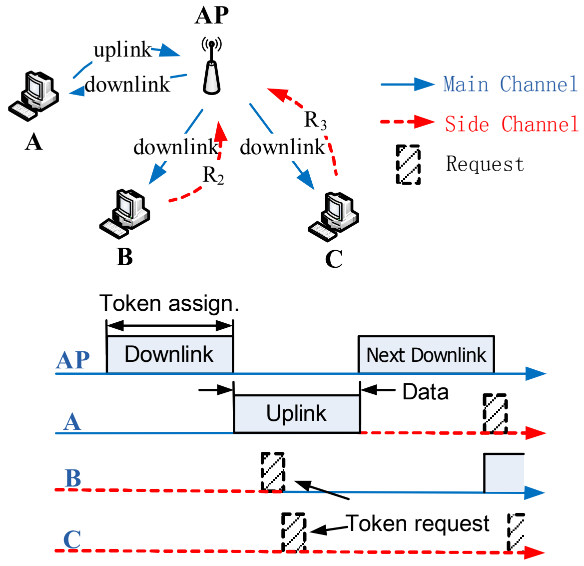

Figure 5: An illustration of DC-MAC operations in time series

4.2 DC-MAC Detail Design

In essential, DC-MAC applies a token-based medium sharing scheme to schedule the communications over Main Channel. The AP assigns the token to a Client who then communicates with the AP. Any token scheduling algorithm is applicable while we apply the simplest round-robin for demonstration purpose. In what follows, we present the DC-MAC in AP and Clients respectively.

It is worth pointing out that as mentioned in Section 3.1, Side Channel is not an appropriate choice when SNR is low. In the DC-MAC protocol, AP is able to calculate the per bit SNR of every packet and decide whether to use the Side Channel mode according to the measured SNR. In the following DC-MAC design, we assume that the SNR is high and the channel condition is good. We will discuss the case when SNR is low or external interference is severe in Section 8.

4.2.1 DC-MAC in AP

The AP will deliver the token management information

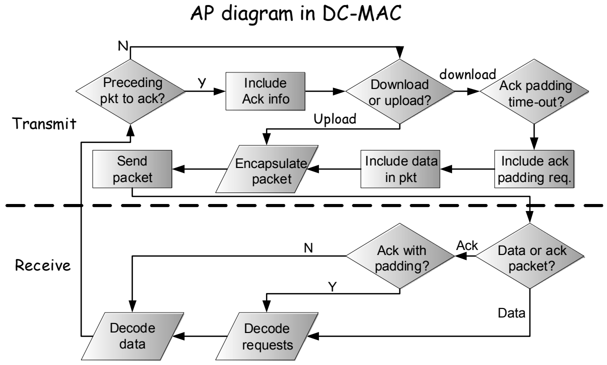

Figure 6: DC-MAC state transition diagram for AP

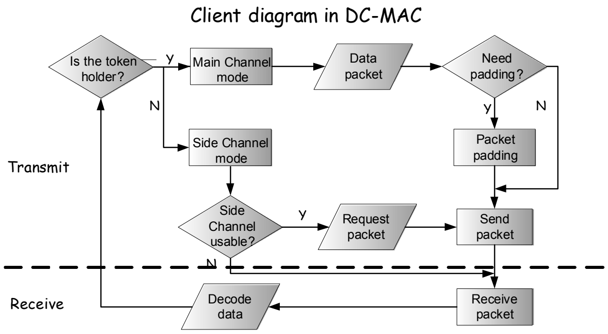

Figure 7: DC-MAC state transition diagram for Clients

in the downlink operation. Each token is valid for one communication only, either upload or download. As long as the instant communication is accomplished, the AP will automatically reclaim the token for the next assignment. In the lost-token scenario, the AP will reclaim the token in a time-out manner. The price for such a scenario is one packet only. Fig. 6 gives the DC-MAC state transition diagram for the AP.

An upload communication starts from the preparation of the downlink operation. The AP first prepares the acknowledgement packet for the previous communication. It then encapsulates the instant downlink packet that carries three parts: 1) the first is the token assignment information so that the expected token holder (Client A in Fig. 5) can obtain the token; 2) the second part is for the non-token holders (B, C in Fig. 5) that carries the specification of the token requests so that they can transmit their upload request (if there is any) through Side Channel; 3) in the last part, the AP appends a synchronization sign so that Clients can be synchronized with the AP. The uplink packet for an upload is much simpler. The AP simply decodes the data in Main Channel and the upload requests in Side Channel.

For a download communication (e.g., A downloads from AP in Fig. 5), it differs from an upload communication in the following aspects. First, AP will notify the instant token holder to pad its uplink packet to a certain length in a time-out manner so that other nodes have the opportunity to send their request. In our configuration, an acknowledgement packet will be mandatorily padded to the 62 bytes so that 31 Clients can be supported by an AP at most. When receiving, AP first checks whether the acknowledgement packet is padded. In a confirmed case, AP will decode Side Channel along with Main Channel. Although 31 clients is enough for typical application scenario, if there are more users to support for some special cases, more intelligent coding scheme can be designed to accommodated that will not discuss here.

4.2.2 DC-MAC in Clients

Upon receiving a downlink packet, a Client first determines whether it is the token holder. If confirmed, the Client enters Main Channel mode and begins to transmit data. In the case of the padding request, the Client pads the acknowledgement as requested. When the Client is not the token holder and has data to send, it will enter Side Channel mode as shown in Figure 7. Before transmitting its request, the Client first checks the availability of Side Channel. Recall Side Channel is available only when it is the upload communication or download communication with a padded acknowledge. For the other case, the Client simply keeps silence. The receiving of the Client is straightforward.

A key issue in DC-MAC is the sending request through Side Channel. Recall that collisions in Side Channel will lead to severe consequence and should be largely avoided. For this we apply a time division scheduling algorithm in Side Channel. Side Channel is partitioned to time slots. Each Client is allocated with one exclusive time slot and sends their request during their time slot.

Clients may join and leave. A Client being inactive for too long time will be kicked out by the AP automatically. To the opposite, a new comer should first listen to the AP's downlink packet. The downlink packet carries the sub-channel utilization information. The new comer simply selects a random un-used time slot to delivers its request. Lost request can be solved by repeat.

Another nice property of DC-MAC design is that, as every node should listen to the packet of the AP and is scheduled by the AP, hidden terminal problem does not exist. It is well known that hidden terminal problem causes severe performance degradation for wireless networks. Though the RTS/CTS mechanism can effectively reduce its occurrence [2] in 802.11, RTS/CTS is not widely adopted because of the huge overhead.

5. IMPLEMENTATION

In this section, we present the implementation of Side Channel and DC-MAC designs. Due to the space limitation, only key issues and challenges during the implementation are highlighted. In the following, we first describe the hardware and software environment for the experiments, and then show the practice of Side Channel and the DC-MAC in detail.

5.1 Platform Configuration

We use GNU Radio [6] as the basic platform to construct our experiment testbed. We apply the IEEE 802.15.4 as the basic network standard since the GNU Radio software project has a mature 802.15.4 PHY layer implementation [27]. Recalling Side Channel exploits the information

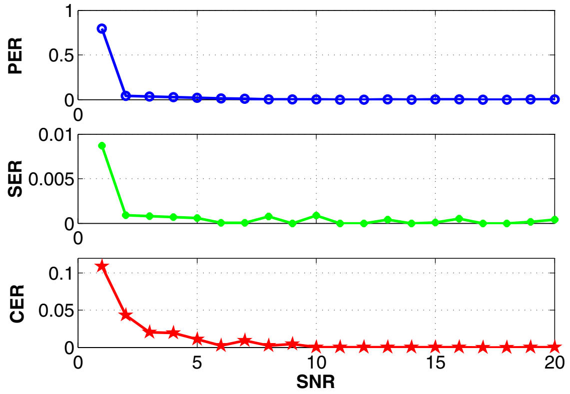

Figure 8: PER, SER and CER of normal transmission under different SNR

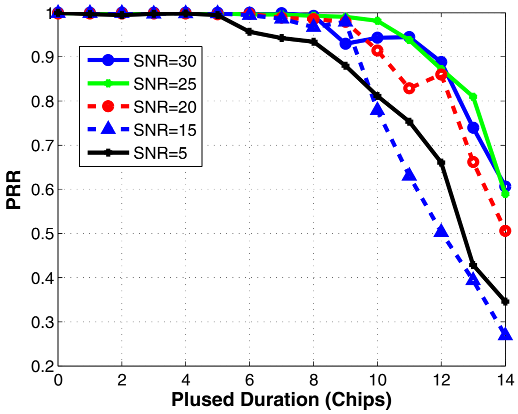

Figure 9: Effect of different duration of interfered chips to Main Channel

from the chip level, the implementation will involves all layer of the network stack.

We employ the Universal Software Radio Peripheral version-2 devices (USRP2) [9] as the hardware platform. Each device is equipped with a XCVR2450 daughterboard for 2.4 and 5 GHz communications, employed as either a transmitter or a receiver. When used as a transmitter, it can have a DAC rate of 400M samples/s while the receiver has the ADC rate of 100M samples/s. For the software part, we are based on an existing work of IEEE 802.15.4 PHY [27], which we adopt and modify to satisfy our experiment requirements.

5.2 Side Channel Implementation

The key issue in Side Channel implementation is to encode information to the intended interference and let it decodable by the receiver. For the transmitter, it first modulates the transmitted information by Pulse-Position Modulation and Pulse-Interval Modulation (PPM and PIM in Section 4). The modulated information is then sent out by a pulsed interference generated by the transmitter. We use timestamp mechanism in USRP2 testbed to achieve chip level synchronization, which will be described in detail in Section 5.3. To guarantee that the chips in a symbol will be affected, we set the duration of pulsed interference to 6 chips. In order to capture the transmission in Main Channel, we set the power of the interference signal twice as the Main Channel transmission power.

Upon receiving a signal, the receiver should decode both the payload in Main Channel and the information in Side Channel. To find out a best-match chip sequence, various methods are possible. We apply one of the most popular ones the maximum likelihood decoder (MLD). For the Side Channel decoder part, it collects the statistics when the MLD decodes the payload [16]. Using an appropriate demodulation method, it can obtain the information in Side Channel.

5.3 DC-MAC Implementation

The key issue in DC-MAC is the synchronization of the different Clients' operation behavior. The key challenge when synchronizing different Client's transmissions is the unpredictable latency in software-defined radio. Upon receiving a packet, an unpredictable latency will be experienced even a response transmitting is immediately issued. This unpredictable latency is mainly affected by the CPU processing time, operation system scheduling delay, and etc. And this unpredictable latency will make the whole DC-MAC protocol fail. To solve this problem, we insert a timestamp on each sample block delivered from the host system to the radio hardware [11]. By this timestamp mechanism, we are able to synchronize the transmission behavior of different Clients. More precisely, for each transmission we add a mandatory delay before the real transmitting. This delay will be long enough to compensate all the uncontrollable latencies. In our experiments, this mandatory delay is set to be 8ms.

As mentioned in Section 4, we use the time division scheduling algorithm in DC-MAC. The interference pattern is set to be within 8 symbols, thus we can support up to 31 nodes if we use the maximum payload as 127 byte in IEEE 802.15.4. We choose PPM to modulate the interference pattern due to its low false negative rate and high capacity which we will show in the evaluation of Side Channel. The duration of pulsed interference is set to 6 chips and we repeat three times for increasing its reliability. Notice that every interfered symbol is followed by a pilot symbol because we may interfere in the between of two chips. At the receiver side, it recognizes any one of the three pulsed induced errors as one request.

6. EXPERIMENTAL EVALUATION

In this section, we use a testbed consisting of eight USRP2 devices to evaluate the performance of Side Channel and DC-MAC. The results demonstrate that the performance degradation of Main Channel is negligible when Side Channel is appropriately used, which well verifies the theoretic analysis. The results also show that DC-MAC performs better than CSMA in all situations, with up to 250% improvement on overall throughput when traffic load is heavy.

6.1 Evaluation of Side Channel

In these experiments, we set three USRP2's acting as Alice (sender), Bob (interferer), and Carol (receiver), respectively. Then, we choose 2.425GHz which is in the worldwide 2.4GHz band as the carrier frequency. In every experi-

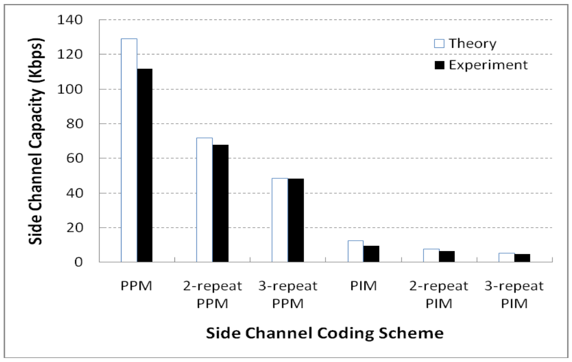

Figure 10: Capacity with different modulation schemes in Side Channel

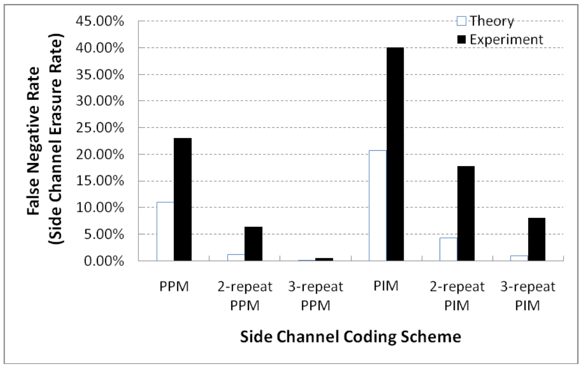

Figure 11: False negative with different modulation schemes in Side Channel

ment below, the sender always continuously transmit IEEE 802.15.4 packets. Each packet consists of 73 bytes (60-byte payload, 11-byte header, and 2-byte checksum), or 146 symbols.

First, to investigate the influence of noise, the interferer is turned off. The value of SNR at the receiver side is carefully tuned to 21 different levels, from 0 dB to 20 dB. For each SNR level, the sender sends 20,000 packets and the receiver records all chip errors, symbol errors, as well as packet losses. We can easily see from Fig.8 that when SNR > 5 dB, packet loss rarely happens, SEP is always lower than 0.2%, and CEP does not exceed 1%. In particular, when SNR > 10 dB, the errors caused by pure noise is negligible even at the chip level.

Second, to investigate the influence of intended interference, the interferer is set to generate various kinds of pulsed interference with different pulse durations. The joint effect of intended interference and noise is illustrated in Fig.9. We find out that if the number of interfered chips with in a symbol is fewer than 8, the performance of Main Channel would not have a significant degradation (less than 5%). This result, along with the result shown in Fig.8, well matches the theoretical conclusion mentioned in Section 3.1. It is worth pointing out that in theory the PRR should be close to 0 when $h = 7$ or 8 since ECC is 6, while in practice the performance is even more desirable. This is because in theory we only considered the worst case that 7 or more chip errors at any positions would lead to symbol corruption, while in reality it is not the case. In other words, our theoretical analysis is very conservative whose conclusion can be safely applied in real situations.

Last, we also evaluate Side Channel in terms of throughput and reliability. As we know, channel coding enhances transmission reliability at the expense of channel capacity. In this experiment, the interferer has 2 options on modulation scheme (PPM and PIM) and 3 options on channel coding scheme (1, 2, and 3-repeat coding). Thus, there are 6 different ways to transmit bits via Side Channel. For each way, we send 1,000,000 symbols at the sender side along with the corresponding intended interference at the interferer side. As shown in Fig.10, in all cases the throughput in the experiment is slightly lower than the channel capacity. We suspect that this is due to the defect of software-defined demodulator. The reliability of Side Channel is measured by the portion of incorrectly delivered bits (false negative rate) which is displayed in Fig.11. For PPM and PIM without repeat coding, the throughput is as high as 129.25 Kbps and 12.39 Kbps, respectively. For PPM and PIM with 3-repeat coding, the false negative rate is as low as 0.48% and 8.02%, respectively. Note that PPM performs better than PIM in terms of both throughput and reliability. However, when chip-level synchronization is not supported by the device, we cannot make use of PPM on Side Channel.

6.2 Performance Evaluation of DC-MAC

We have shown that Side Channel has adequate capacity and reliability for transmitting a small amount of data. The remain part of this section will compare the performance of DC-MAC which exploits Side Channel with CSMA. We implement prototypes of both DC-MAC and CSMA on the same platform (GNURadio and USRP2). We use 1 USRP2 as AP and up to 7 USRP2 as users. In addition, our implementation of DC-MAC uses 3-repeat PPM as the Side Channel modulation and coding scheme.

We investigate the overall network throughput when the number of user nodes varies. In our test bed, each user node can send at a maximum speed of 62 packets per second (i.e., no waiting time). It takes around 8 ms to transmit a packet at the sender side or to transmit an ACK at the AP side. Hence, it takes around 16 ms to deliver a packet in a round trip. As a result at most 1000/16=62.5 packets can be sent in one second. Fig.12 shows the overall throughput when the packet rate of each node is fixed to 31 packets per second which is half of the maximum speed. Fig.13 shows system throughput under a saturation condition: every device always has a packet to transmit. We can see that DC-MAC outperforms CSMA in all cases. We also see that as the number of users increases, the performance of CSMA could decrease dramatically due to transmission collisions, while the performance of DC-MAC degrades gracefully since it is completely collision free and all packet losses are induced by intended interference. However, the packet loss in this experiment seems worse than that shown in Fig.11. We suspect that this is also because of the drawbacks of software-defined signal processing. Even when there is only 1 user and therefore CSMA will not have any packet collision, the extra back-off time and carrier sensing overhead also make it slower than DC-MAC. In both cases, DC-MAC has up to 250% performance gain (7 users) against CSMA in terms of overall throughput. We further compare the throughput when the number of users is fixed to 7 but the overall traffic load varies. The result is shown in Fig.14.

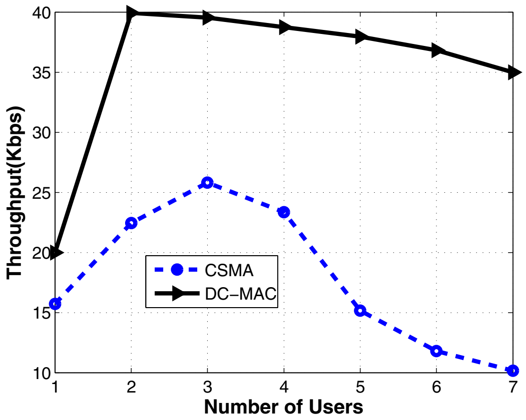

Figure 12: DC-MAC performance in an unsaturated network

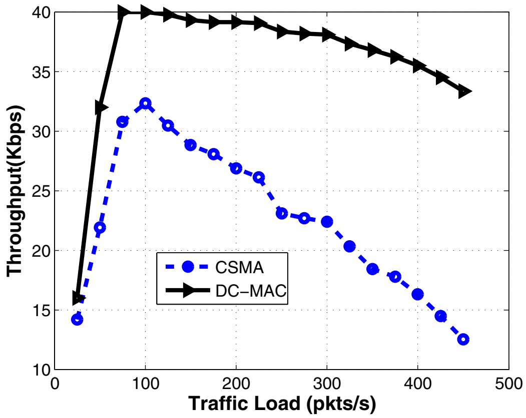

Figure 14: DC-MAC performance under different traffic loads

Additionally, Fig.15 unveils the major reason why DC-MAC could easily outperform CSMA. A large portion of packets are corrupted by collision in CSMA. DC-MAC does not share the same problem since it always suppresses packet sending at the user side unless the AP asks it to do so. In this figure, we find out that the packet loss rate drops seriously when traffic load increases. We believe it is because of the increasing interference which will likely induce more packet loss. In our experiment, the maximum packet loss rate of DC-MAC is 16.61%. We believe that a much lower packet loss rate could be achieved by designing a more robust demodulator.

7. RELATED WORK

Interference has been a hot research topic in wireless communication for a long time. Previous works fall into the following two categories.

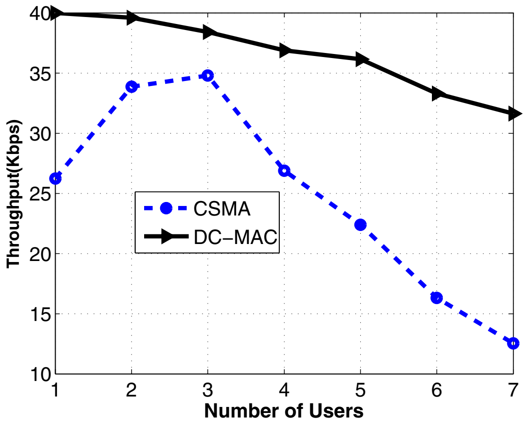

Figure 13: DC-MAC performance in a saturated network

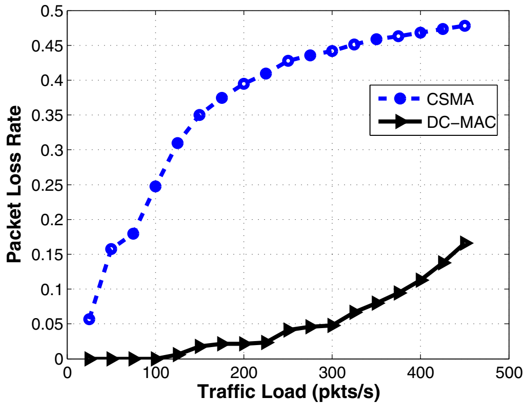

Figure 15: Packet loss rate of DC-MAC and CSMA under different traffic loads

7.1 Interference management:

The first category of interference management can be further divided into three sub-categories.

- Interference avoidance: Multiple access techniques allow multiple transmissions at the same time in the context of single-antenna such as CDMA [23], FDMA [8], and spatial reuse [8]. Some designers attempted to prevent interference by distributing the resources to users. In effect, the channel capacity will be divided. For instance, different users might obtain different frequency bands [15, 24, 31], different codes [22, 23] or time slices [17]. These approaches tried to prevent the interference, while our work attempt to use the interference to deliver information.

- Interference cancellation: Wireless network coding is also a hot topic in recent years. Some designers use interference cancellation technique to decode in the presence of interfered signals [7, 29], aiming at recovering certain amount of error packets. Analog network coding [26] is a work related to us since signal is mixed in the air not the router, which is different from the traditional wireless network coding [25, 30]. They treat the interference as communication barriers and try to recover the interference-induced errors. IC is also used for convey side information, i.e. AP cancels main frame and gets the side channel information. It is known as Rate (power) split channel access [5]. In our work, we leverage those interference-induced errors to deliver coordinate information.

- Interference alignment: In IAC [29], Katabi et. al coordinate the information among multiple receivers in order to overcome the antennas-per-AP throughput limitation. In these works, however, the effective gain for each individual antenna keeps the same, while the gain is from the accumulating throughput of more antennas. In our work, we are targeting to improve the MAC performance by improving the throughput of each individual antenna. In a multiple antenna scenario, such improvement will be accumulated.

7.2 Coordination Scheme

The traditional coordination schemes can be divided into two categories, the in-band and out-of-band approaches. The out-of-band coordination is suitable for multiple radio scenarios. In these approaches (e.g., [10]), one radio/channel is dedicatory allocated for coordination, and the other radios/channels are used for data transmission. This coordination radio/channel will therefore be wasted, providing no gain for the network throughput.

For the in-band approaches (e.g., [3]), the coordination traffic are within the same channel of the data traffic. There are two typical in-band coordination schemes, CSMA and TDMA, both of which have certain inherent disadvantages. CSMA will bring a large amount of communication overhead for the system. For example, DIFS, SIFS and random back-offs in CSMA waste a lot of capacity in particularly when channel condition is good. In a recent research, Brodsky et.al [21] claimed that CSMA was able to achieve near-optimal average throughput in common network environments. They, however, also pointed out that the claim was valid only in point-to-point scenario. The claim could not hold in a large scale network where the coordination cost would be dominating. On demand of this, we design the free Side Channel for coordination purpose and develop the DC-MAC to use it.

TDMA allows several users to share the same frequency channel by dividing the signal into different time slots. The users transmit in rapid succession, one after the other, each using its own time slot. One major disadvantage of TDMA technology is that the users have a predefined time slot. If some clients do not have data to send, the time slots will be waste. In our DC-MAC, Side Channel is using TDMA to guarantee the collision-free on Side Channel (recall that collisions on Side Channel will severely affect the Main Channel throughput). Nodes request Main Channel throughput in Side Channel, and access Main Channel to finish the transmission. As such Main Channel is accessed in an on-demand manner, wasting no communication resources while TDMA will waste because of the under-utilized time slots.

8. DISCUSSION

In this section, we will discuss some issues in our current Side Channel design and give a potential method to extend the Side Channel concept to more general standards based on other physical layer techniques.

Currently, our Side Channel design is implemented based on IEEE 802.15.4 which is DSSS-based. For the non-DSSS-based standards, e.g. 802.11a/g/n (OFDM based), the design is much more challenging and can be done using following techniques. First, we send the information in Side Channel by generating certain predefined interference patterns. However, instead of using the chip error information which is achieved by the decoder, we will use energy detection to reliably record the interference signals when sampling the received signals. Since the interfered signal will have much higher amplitude than the original ones, we can set a threshold and record all signals exceed this threshold. We record the analog interference signals before decoding the received signals. And we will use this information to build a Side Channel. Next, we can use interference-free bits to estimate the channel distortion. After that, we can combine the channel coefficient and the interference information to recover the original data directly. Actually, it is a more general technique that can be applied to other modulation algorithms.

In the practical wireless environment, the external interference is unavoidable and the channel condition will be poor when it happens. Under such scenarios, we can still use Side Channel when the link is not pushed to the limit as shown in Figure 4. Our current design leverages the redundancy of coding scheme and will sacrifice some anti-interference ability. As mentioned before, we will extend to OFDM by using energy detection and interference cancellation technique. In that case, our Side Channel design will not base on the redundancy of coding scheme and thus can handle the external interference as normal.

Our work may also extend from a single network scenario to multiple APs scenarios. The current DC-MAC and Side Channel implementation are modulated using PPM and PIM as mentioned in Section 3. These are two simple yet illustrative modulation schemes. By designing more efficient modulation schemes, we can encode the destination ID into Side Channel. In that case, our DC-MAC can work under multiple APs scenarios.

9. CONCLUSIONS AND FUTURE WORK

In this paper, we present our observation on interference patterns. We use special designed interference patterns to build a free in-band Side Channel without degrading the effective throughput of Main Channel. We analyze the capacity of Side Channel and propose DC-MAC to fully exploit its advantages. As the coordination among multiple users becomes free, the Main Channel utilization efficiency can be dramatically increased. USRP2-based implementation experiment showed compared with the CSMA-based approaches, DC-MAC improves the network throughput by up to 250%.

The design of Side Channel envisions a new paradigm of communications. A receiver with a single antenna is allowed to receive multiple transmission sessions at the same time. Along this direction there are many new issues and challenges to be addressed.

We developed two modulation schemes for Side Channel, and more efficient modulation schemes are possible under different hardware constraint. We designed DC-MAC for infrastructure-mode only, how to design an efficient MAC protocol for ad hoc model remains an interesting problem. The hidden terminal problem in DC-MAC is indeed challenging and actually this is one of our on-going investigations. All these can be good topics for our future work.

10. ACKNOWLEDGEMENTS

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